Remarks

Reconsideration and withdrawal of the outstanding rejection to the claims, in consideration of this Amendment, is respectfully requested.

The accompanying Substitute Specification corresponds to the originally filed Substitute Specification with regard to prior, parent U.S. Application Serial No. 10/400,469, filed March 28, 2003. The continuing data information on page 1 of the Substitute Specification incorporates the continuing data information entered in connection with the Preliminary Amendment filed on even date with the filing of the above-identified present application. Since the originally filed Substitute Specification was previously officially entered into the record of the parent application and was accompanied with a marked-up version thereof, a marked-up version with regard to the present submission of the Substitute Specification is not being submitted herewith. It is submitted, new matter is not being added with regard to the Substitute Specification, either by addition and/or deletion. Acceptance therefor of the Substitute Specification (enclosed herewith as **Appendix A**) as a replacement of the originally filed Specification is respectfully requested.

Applicants note with appreciation the allowance of claims 63-67 and 71-74.

By the above-made amendments, claims 52-57, 63-67, 71-74 and 86-150 are pending of which claims 52, 54, 55, 57, 63, 71 and 74 were amended and claims 86-150 are newly presented. Independent claim 52 as well as dependent claims 54 and 55 were amended for purposes of effecting further clarification of the invention set forth therein. Additional revisions of a minor formal nature were effected, also, in independent claim 52 and corresponding dependent claim 57 as well as in both of allowed independent claims 63 and 71. The latter changes were implemented in order to conform like expressions employed throughout the body of the individual

claims, clearly not effecting the substantive nature of the claims. For example, the expression "first (second) conductive pattern" was amended to the expression first (second) conductor pattern. Throughout the presently pending claims expressions such as "first conductive film" and "second conductive film" along with "first conductor pattern" and "second conductor pattern" are featured. An example of the "first conductive film" can be seen with regard to the polysilicon film 48, 49 in Fig. 19 of the drawings and discussed on page 66 of the Substitute Specification. Likewise, the "second conductive film" can be seen with regard to the n-type and p-type polysilicon films 56 and 57, respectively, with regard to Figs. 22+ and discussed on page 68 et seq. of the Substitute Specification. Since the revisions implemented in allowed claims 63, 71 and 74 include improving the readability thereof, acceptance of the same as well as a reaffirmation of allowance of those claims along with their corresponding dependent claims thereof, is respectfully requested.

In addition to effecting further clarification of the set forth featured aspects according to independent claim 52, an insertion was also implemented therein relating to the formation of the silicide layers on the respective first and second gate electrodes of the memory cell. This will be further discussed with regard to the rebuttal arguments to the outstanding art rejection.

According to the outstanding Office Action, claims 52-57 stand rejected under 35 USC §102(b) as anticipated by Shimizu et al (USP 6,555,427 B1). As will be shown hereinbelow, the invention according to claims 52-57 and also with regard to the newly presented claims was neither disclosed nor would have been suggested from Shimizu et al. Therefore, this rejection is traversed and reconsideration and withdrawal of the same is respectfully requested.

The invention according to independent claim 52 is a method of manufacturing a semiconductor integrated circuit device which comprises the steps of:

forming a first conductive film over a memory cell forming region and a peripheral circuit forming region of a semiconductor substrate (e.g., see the non-doped polysilicon film 48 and the n-type polysilicon film 49 in Fig. 19 of the drawings and the related discussion on page 66 of the Substitute Specification);

patterning the first conductive film in the memory cell forming region to form a first conductor pattern which serves as a first gate electrode of the memory cell (e.g., see the discussion on page 66 and Fig. 20 of the drawings which shows the patterning of the first conductive film in the memory cell forming region into a conductor pattern 51 covered by silicon nitride insulator 50 in connection with the formation of a first gate electrode such as 3 in Fig. 1 and 51 in Fig. 20 etc.);

forming a second conductive film (e.g., 56, 57) over the memory cell forming region and over the first conductive film in the peripheral circuit forming region (e.g., see Fig. 22 and the related discussion on page 68);

etching the second conductive film (e.g., 56, 57) so as to form a second gate electrode of the memory cell on at least side surface of the first conductor pattern (e.g., 51), and to form an electrode structure of a peripheral circuit element comprising the second conductive film and the first conductive film in the peripheral circuit forming region (e.g., see Fig. 23 and the related discussion on page 69); and

forming a first silicide layer on the first gate electrode of the memory cell and a second silicide layer on the second gate electrode of the memory cell (e.g., see silicide layers 14 which are on the first and second gate electrodes 3 and 8, respectively, with regard to Figs. 2 et seq. and likewise see silicide layers 77 which

are on the first and second gate electrodes 51 and 62, respectively, in the memory cell forming region of Fig. 27, et seq.).

Dependent claims 53 et seq. thereof further characterize the structurally defining aspects directed to the method of manufacture according to claim 52. For example, the first gate electrode which constitutes to control gate electrode of the memory cell forming region can be seen by gate electrodes 3 or 51 in the drawings and the second gate electrode of the memory cell which constitutes the memory gate electrode can be seen with regard to the memory gates 62 (8, 27 and 200) in the drawings which is disposed over the channel region, the charge storage region being formed between the channel region and the memory gate electrodes, as can be seen with regard to Figs. 1, 2 et seq. of the drawings. Regarding the memory gates 62, for example, it is noted that the formation thereof is on at least side surface of the first conductor pattern and is described, on page 69, of the Substitute Specification as being formed as a side spacer-like memory gate 62 on side walls of the first gate film patterns 50 and 51 in regions uncovered with the second gate film patterns 193 through the insulating film 4, silicon nitride film 6 and CVD oxide film 7 on a self-alignment basis with respect to the first gate film patterns 50 and 51 (see also laminated insulating film 54 in Figs. 21-23 as well as claim 55 et seq.). It is submitted, the invention as now set forth in independent claim 52 and further according to the corresponding dependent claims thereof not only could not have been anticipated by Shimizu et al but, moreover, could not have been suggested therefrom.

Shimizu et al disclosed a non-volatile memory cell technique including a stacked gate structure of a double-layer with regard to effecting memory miniaturization. Figs. 30A-30B and 32A-32D represent example techniques

disclosed by Shimizu et al, which are discussed in column 26, line 62 et seq. and column 27, line 45 et seq. thereof. As can be seen from these and other examples in Shimizu et al, the stacked-gate structure of a double-layer lower layer gate (e.g., layers 83 and 87 for low-voltage application or layers 83 and 97 for high-voltage application) correspond to a floating gate 47 such as shown in Fig. 30B and discussed, for example, on column 27, line 52, to column 28, line 7, in Shimizu et al. It is submitted, Shimizu et al neither disclosed nor suggested, for that matter, a scheme as that set forth in currently amended claims 52+ which call for, amongst the featured aspects therein, a silicide process with regard to the double-layer. Shimizu et al, it is submitted, also did not disclose or suggest a memory cell having a sidewall spacer type gate electrode such as the memory gate 8 in Figs. 1 and 2 and memory gate 62 in Fig. 27 et seq. which are examples thereof according to the present invention. As can be seen from Figs. 2 or 27 of the drawings in the present application, although not limited thereto, the silicide layers such as 14 and 77 are formed on both the first gate electrode (e.g., 3, 51) and the second gate electrode (e.g., 8, 62) of the memory cell (see the earlier discussion in these remarks directed thereto). For at least the above reasons, the invention according to independent claim 52 as well as the corresponding dependent claims thereof could not have been anticipated nor, for that matter, realizable from Shimizu et al's teachings.

The above discussion regarding example aspects featured in the various example embodiments described and illustrated in the present application, which relate to the above-discussed claims 52+, is also applicable with regard to various inventive aspects recited in each of the newly added independent claimed groupings covered by claims 86-150. In this regard, it can be seen from Fig. 27 et seq. of the drawings, although not limited thereto, that the silicide layers forming step further

includes the formation of a silicide layer such as a "third silicide layer" on the second conductive film of the electrode structure. This can be seen with regard to silicide layers 14 or 77 which are formed on the gate electrode structure of the PMOS and NMOS transistors in the peripheral circuit forming region such as shown in Fig. 27 of the drawings (see claim 86). Additional details regarding the silicide layers forming step are covered with regard to newly added dependent claims 139-150. Also, it is submitted, each of the newly added claim groupings, including claims 87+, 89+, 90+, 91+, 98+, 101+, 104+, 105+, 110+, 113+, 123+, 127+, 131+ and 135+, are characterized by a manufacturing scheme of a semiconductor integrated circuit device featuring the formation of the first and second gate electrode associated with the memory cell structure as well as the silicide layers forming steps such as that contained with regard to independent claim 52 as well as with regard to the earlier allowed claims 63+ and 71+, although presented in a somewhat modified form therefrom. For the same and similar reasons as that discussed above, the method of manufacture according to the newly presented claims could not have been anticipated or suggested from Shimizu et al.

Therefore, in view of the amendments presented hereinabove, reconsideration and withdrawal of the outstanding rejection as well as favorable action on all of the presently pending claims, i.e., claims 52-57, 63-67, 71-74 and 86-150, and an early formal notification of allowability of the above-identified application is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including Extension of Time fees, to the Deposit Account of

Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (501.42645VX1), and please credit any excess fees to such deposit account.

Respectfully submitted,
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APPENDIX A